Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor integrated circuit, comprising:

a plurality of selectable pathways inter-connected between a plurality of data sources and data destinations;

a cryptographic circuit connected to the selectable pathways and arranged to selectively receive data at an input from at least one of the data sources, to decrypt or encrypt the data in accordance with a key, and selectively provide the encrypted or decrypted data to at least one of the data destinations via an output;

an instruction ~~interpreter~~ circuit arranged to receive ~~as an~~ on a first input an instruction signal and to generate therefrom an output to control the plurality of selectable pathways to select a data pathway configuration of the circuit, thereby selecting from which of the data sources the cryptographic circuit receives data and to which destination the cryptographic circuit provides the data;

wherein the instruction ~~interpreter configured such that the instruction signal defines~~ circuit is configurable by a ~~data~~ pathway configuration ~~of the system, and such that it operates~~ limiting rule signal, received at a second input, to operate in accordance with ~~a~~ the rule signal that limits the data pathway configurations ~~which~~ that are selectable by the instruction signal, thereby limiting the flow of data between the data sources and data destinations.

2. (Currently Amended) The semiconductor integrated circuit of claim 1 wherein the ~~instruction interpreter is arranged to receive~~ a rule signal ~~defining~~ defines those data pathway configurations that are unselectable.

3. (Currently Amended) The semiconductor integrated circuit of claim 2 wherein the rule signal is chosen from a plurality of ~~possible~~ rule signals according to a mode of operation of the system.

4. (Currently Amended) The semiconductor integrated circuit of claim 3 wherein the plurality of rule ~~signal is~~ signals are generated by a rule selector, and wherein the rule selector comprises a plurality of anti-fuses allowing one of a plurality of selectable configurations to be chosen.

5. (Original) The semiconductor integrated circuit of claim 4 wherein each of the anti-fuses can be configured once only.

6. (Original) The semiconductor integrated circuit of claim 1 wherein the instruction signal is generated by a CPU.

7. (Currently Amended) The semiconductor integrated circuit of claim 6 wherein the CPU is arranged to generate ~~an~~ the instruction signal comprising an instruction portion and a data portion.

8. (Original) The semiconductor integrated circuit of claim 1 wherein the instruction signal and rule signal are 32-bit data fields.

9. (Original) The semiconductor integrated circuit of claim 1 wherein the plurality of data sources and destinations includes at least one memory for storing encryption or decryption keys.

10. (Original) The semiconductor integrated circuit of claim 1 wherein the key is selected from a plurality of keys in dependence on the instruction signal.

11. (Original) The semiconductor integrated circuit of claim 10 wherein the key is selected from one of a plurality of key stores and provided to a key input of the cryptographic circuit in dependence on the instruction signal.

12. (Original) The semiconductor integrated circuit of claim 10 wherein the cryptographic circuit has a key input, and the key provided to the key input is selected in accordance with the selected pathway.

13. (Original) The semiconductor integrated circuit of claim 1 wherein the circuit is arranged to descramble television broadcast signals using a series of control words.

14. (Original) The semiconductor integrated circuit of claim 1 wherein the circuit is arranged to decrypt encrypted control words using a service key.

15. (Original) The semiconductor integrated circuit of claim 1 wherein the circuit is arranged to decrypt encrypted service keys using a secret key.

16. (Original) The semiconductor integrated circuit of claim 1 wherein the circuit is arranged to perform memory-to-memory transfers.

17. (Original) The semiconductor integrated circuit of claim 12 wherein the plurality of selectable pathways are configurable such that when the data from the data source is a service key, the cryptographic circuit receives a secret key at the key input.

18. (Currently Amended) The semiconductor integrated circuit of claim 12 wherein the plurality of selectable pathways are configurable such that when the data source is a memory and the data destination is a memory, the cryptographic circuit ~~(9)~~ receives a software written key at the key input.

19. (Original) The semiconductor integrated circuit of claim 12 wherein the plurality of selectable pathways are configurable such that when the data source is a plurality of control words, the cryptographic circuit receives a service key at the key input.

20. (Original) The semiconductor integrated circuit of claim 12 wherein the plurality of selectable pathways are configurable such that when the data source is broadcast data, the cryptographic circuit receives a software written key at the key input.

21. (Original) The semiconductor integrated circuit of claim 9 wherein one of the key memories stores at least one key generated by a software algorithm.

22. (Original) The semiconductor integrated circuit of claim 9 wherein one of the key memories stores at least one service key for decrypting control words.

23. (Original) The semiconductor integrated circuit of claim 9 wherein one of the key memories stores a secret key for decrypting service keys.

24. (Original) The semiconductor integrated circuit of claim 1 wherein the plurality of data sources and destinations includes at least one of a hard disc, ROM, RAM, data in port and data out port.

25. (Original) The semiconductor integrated circuit of claim 1 wherein the cryptographic circuit is an AES circuit.

26. (Currently Amended) The semiconductor integrated circuit of claim 1 wherein the plurality of selectable pathways are selected by at least one ~~multiplexor~~ multiplexer or switch.

27. (Currently Amended) The semiconductor integrated circuit of claim 1 wherein the instruction ~~interpreter~~ circuit comprises a plurality of combinatorial components arranged such that the output is generated as a function of the instruction signal.

28. (Currently Amended) The semiconductor integrated circuit of claim 1 wherein ~~the~~ an encryption system is a subscriber-based pay-television system.

29. (Currently Amended) The semiconductor integrated circuit of claim 1 wherein ~~the~~ an encryption system is a monolithic integrated circuit.

30.-37. (Canceled)

38. (New) A method of configuring a circuit in an encryption system in which data is routed between a plurality of data sources and data destinations along a plurality of selectable pathways inter-connected between the data sources and data destinations, the method comprising the step of configuring a rule selector to generate a pathway configuration limiting rule signal defining a rule specifying those data pathway configurations of the circuit that are unselectable.

39. (New) The method of claim 38 in which the rule selector comprises one or more anti-fuses, each anti-fuse comprising a switch arranged to output an electrical signal of 0 or 1 according to the configuration of each anti-fuse, in which each anti-fuse can be configured once only, and in which the pathway configuration limiting rule signal comprises the output of the anti-fuses, and in which the step of configuring the rule selector comprises the step of configuring one or more of the anti-fuses.

40. (New) The method of claim 38 in which the rule selector comprises a one-time-programmable memory and in which the pathway configuration limiting rule signal comprises the output of the one-time-programmable memory, and in which the step of

configuring the rule selector comprises the step of storing a value in the one-time-programmable memory.